DATA-CONTROL SYSTEMS, INC.

INSTRUCTION MANUAL

MODEL SDC-9
FREQUENCY TRANSLATOR

2

103

INSTRUCTION MANUAL

MODEL SDC-9
FREQUENCY TRANSLATOR

2

This instruction manual consists of the following pages:

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ERRATA
MODEL SDC-9

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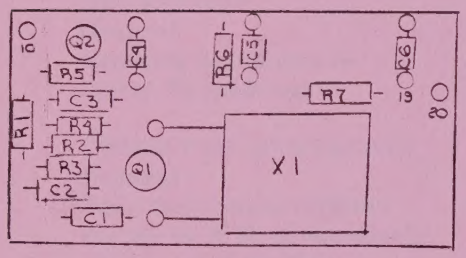
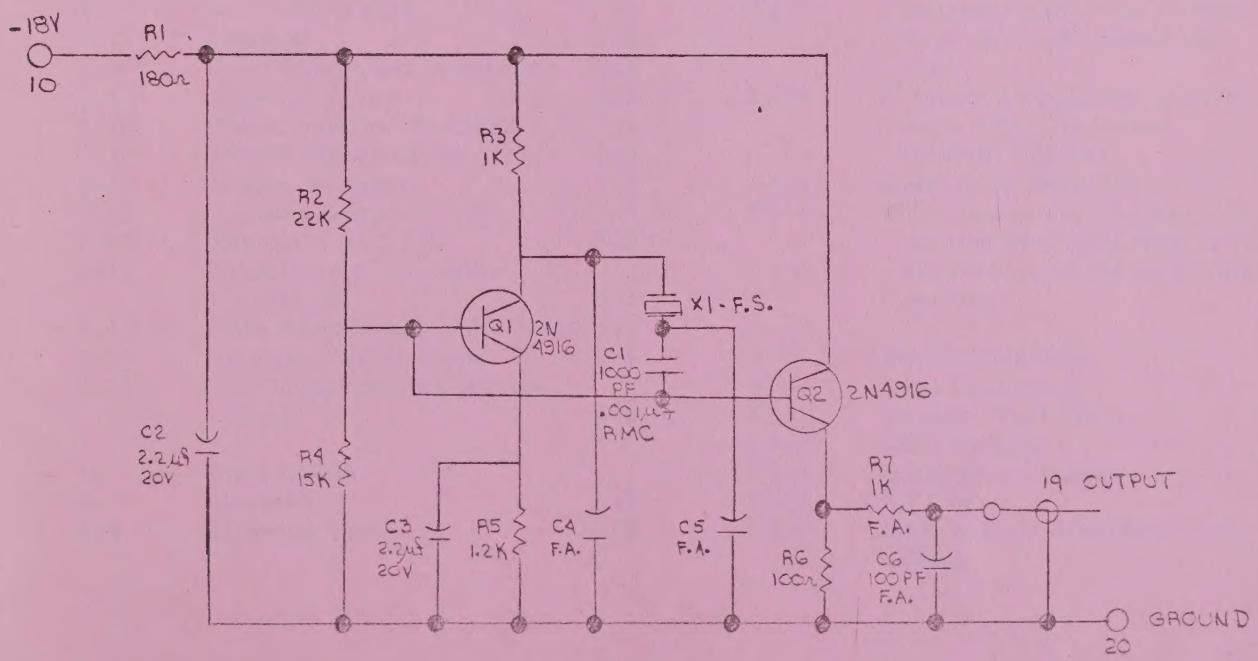
Replace drawing #756429 in Section VI with drawing #758336 shown below.





F.A. = FACTORY ADJUST
F.S. = FREQUENCY SENSITIVE

CRYSTAL OSCILLATOR BOARD
ASSEMBLY #758336

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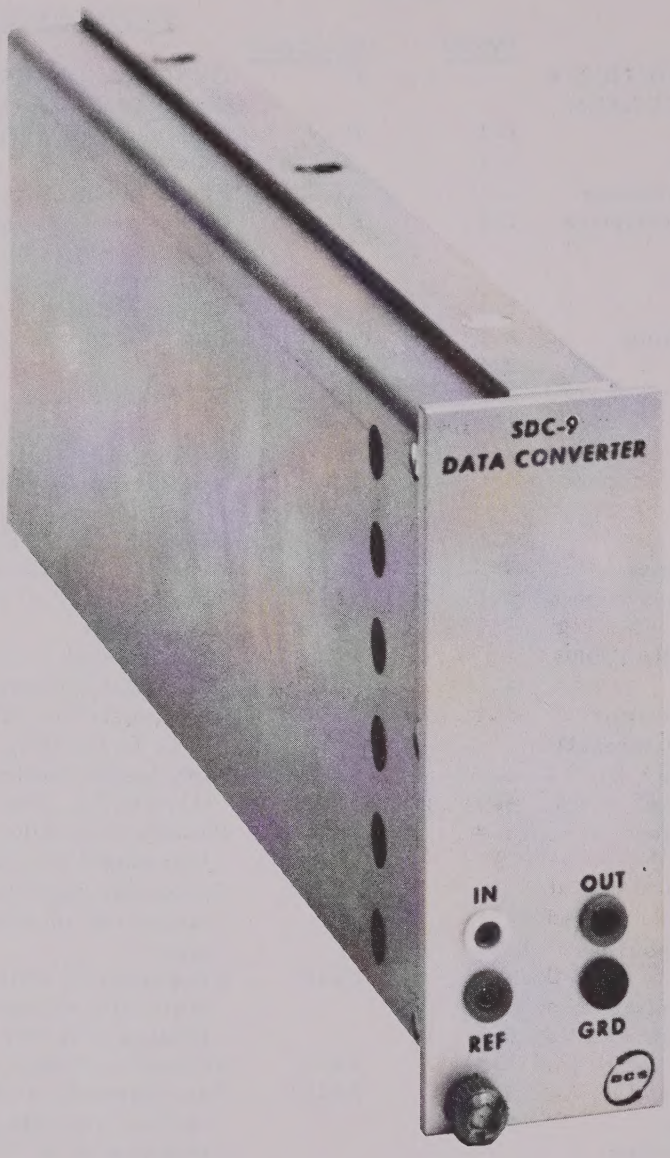


Figure 1-1. SDC-9, Frequency Translator.

SECTION I
GENERAL DESCRIPTION & LEADING PARTICULARS

1-1. GENERAL.

1-2. The DCS Model SDC-9, Frequency Translator, is a flexible, general purpose, double balanced modulator that may be used as a frequency up or down translator, amplitude demodulator, a 0° to 180° phase shift keyed modulator, phase detector, FM detector or a frequency doubler.

1-3. Auxiliary hardware such as crystal oscillators, low pass filters and high pass filters may be incorporated into the basic SDC-9.

1-4. The SDC-9 in its simplest configuration consists of a balanced modulator utilizing an external reference frequency. By entering the device on connector Pin 11 and introducing a data frequency through Pin 1, the resultant heterodyned frequencies will then be available at the unit's output on Pin 19. Crystal controlled reference frequencies may be added within the unit for applications requiring a precision trans-lation reference frequency. Up to 11 internal crystal reference frequencies controlled by a front panel switch are available. Internal seven pole, elliptic function high pass or low pass filters may be connected to the input and the output of the SDC-9.

1-5. MODEL NUMBERING.

1-6. The basic model and the available options are defined as follows.

1-7. Basic unit is the Model SDC-9, Frequency Translator.

1-8. The reference input impedance is defined by a single digit following the basic model number. The SDC-9-1 has a reference input impedance of 100 ohms. The SDC-8-2 has a reference input impedance of 1000 ohms.

1-9. The internal reference tones are defined by a two digit number following the basic model number with an R or RM added. The SDC-9-RXX or SDC-9-RMXX(with front panel manual control) substitute digits for the Xs to define the number of crystals.

1-10. The filter model numbers are shown in Table 1-1.

Table 1-1. Filter Model Numbering.

Filters	Input	Output
Low Pass	SDC-9-L1	SDC-9-L2
High Pass	SDC-9-H1	SDC-9-H2
Bandpass	SDC-9-B1	SDC-9-B2
Reference Bandpass	SDC-9-B3	

1-11. Thus an SDC-9-L1-L2 is a frequency translator with an input and output low pass filter. An SDC-9-R08 is a frequency translator with 8 crystals (in this instance all reference tones desired must be specified when ordering). An SDC-9-2-B3 is a frequency translator with 1000 ohms reference input impedance and a reference input bandpass filter.

1-12. PHYSICAL CHARACTERISTICS.

1-13. The SDC-9 is designed to mount in a single module space of the DCS Model GMA, Module Assembly/Power Supply, from which it derives all power, cooling and signal interconnection. It is contained in an aluminum chassis which measures 1.14" (2.9 cm) wide x 3.29" (8.37 cm) high x 10.5" (26.67 cm) long and wieghs approximately 1 pound.

1-14. ELECTRICAL CHARACTERISTICS.

1-15. The electrical characteristics of the SDC-9 are given below:

Data Input
Frequency Range: 1 kHz to 7 MHz.
Voltage Level: Adjustable 160 millivolt RMS to 3V RMS nominal.
Impedance: 500 ohms nominal (may be matched to line impedance with terminating resistor).

Reference Input
Frequency Range: 100 kHz to 10 MHz (lower input frequencies available on special order).
Voltage Level: 300 millivolts RMS to 1V RMS.
Impedance: 250 ohms nominal (may be matched to line impedance with terminating resistor).

Data Output
Frequency Range: DC to 5 MHz ±3 dB.
Output Voltage Level: 1V RMS for reference frequencies up to 200 kHz. Recommended output level for reference frequencies in range from 200 kHz to 10,000 kHz may be determined as:

$$V_{pp\ out} = 20 \left[\frac{1}{f_{kHz}}\right]^{1/3}$$

Impedance: 50 ohms, nominal.
Output Spurious Level: All data feedthrough components at least 40 dB down from data input.
Reference Carrier Components:

100 kHz to 500 kHz reference	= -40 dB
above 500 kHz to 1 MHz reference	= -35 dB
above 1 MHz to 2 MHz reference	= -30 dB
above 2 MHz to 10 MHz reference	= -20 dB

Internal Reference
Up to 11 crystal controlled frequencies may be provided within a single unit. Control may be from front panel or remote.

Frequency Range: 100 kHz to 10 MHz.
Accuracy: ±.01%.
Stability: 3 parts per million (.003%) per degree C over a 30 ±20°C temperature range.

Low Pass Filter:
Characteristics: Seven pole, elliptic function.
Ripple: Less than ±0 5 dB within band.
Attenuation: Greater than -35 dB at 1.2 times the -3 dB point.
Connection: May be placed on input or output depending on application requirement. (2 may be contained within a single unit.)

High Pass Filter
Characteristics: Seven pole, elliptic function.
Ripple: Less than ±0.5 dB within band.
Attenuation: Greater than -35 dB at 0.8 times the -3 dB point.
Connection: May be placed on input or output depending on application requirement. (2 may be contained within a single unit.)

Bandpass Filter
Characteristics: Combination of 7 pole, elliptic function low pass filter and high pass filter provides an extremely sharp cutoff bandpass filter that may be utilized on the input or output of the balanced modulator.

Power Supply Requirements
Voltages: ±18V.
Power: +18V at 150 mA. -18V at 70 mA.

1-16. Elco pin connections and their functions are given in Table 2-1 on page 1-3.

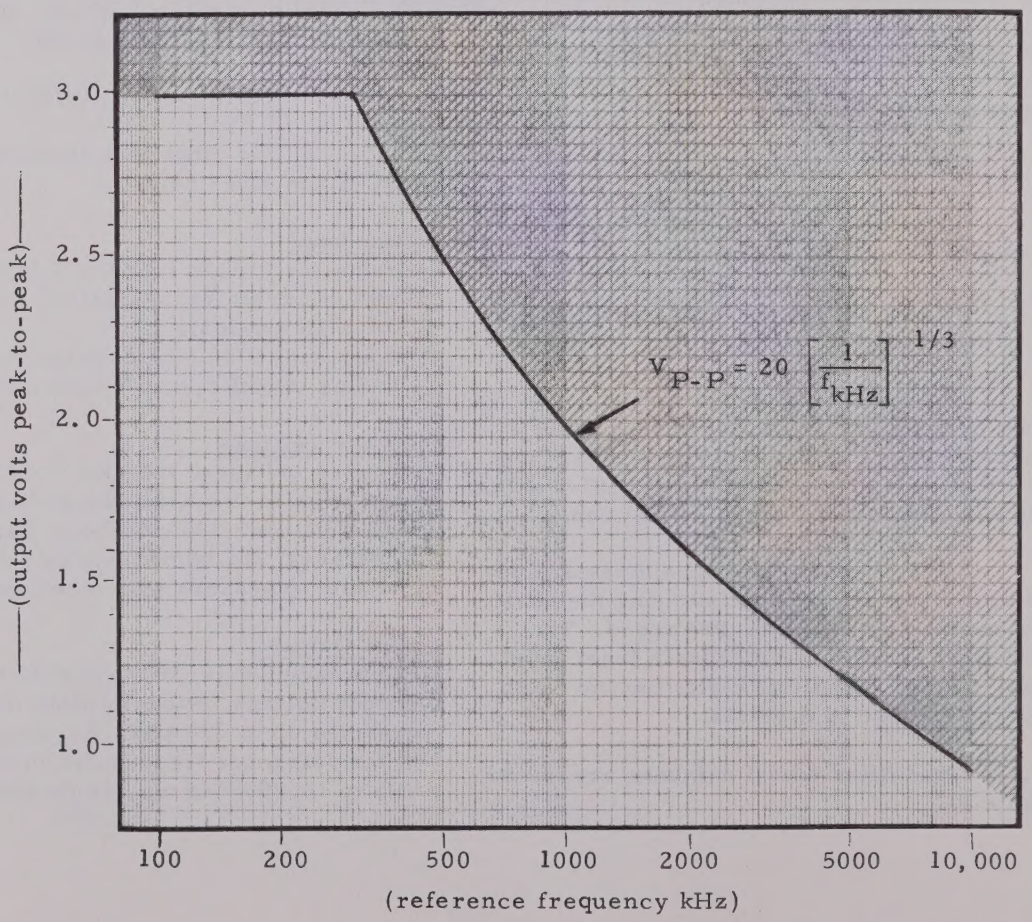


Figure 1-2. Output peak-to-peak Voltage Levels (as function of reference carrier frequency).

Table 1-2. Elco Pin Connections.

Pin #	Description
1(top)	Data Input
2	Data Input Ground
3	Ref. #1* Program
4	Ref. #2* Program
5	Ref. #3* Program
6	Ref. #4* Program
7	Ref. #5* Program
8	Ref. #6* Program
9	+18VDC
10	-18VDC
11	Reference Input
12	Reference Input Ground
13	Ref. #7* Program
14	Ref. #8* Program
15	Ref. #9* Program
16	Reference Output
17	Ref. #10* Program
18	Ref. #11* Program
19	Data Output
20(bottom)	Data Output Ground

* Wired only when reference oscillators are included in unit.

SECTION II
INSTALLATION

2-1. GENERAL.

2-2. This section covers the procedure for installation of the unit prior to operation.

2-3. UNPACKING & HANDLING.

2-4. The unit is sealed in a moisture proof packing material and insulated to absorb shock during shipment. There are no accessories or hardware packed with the equipment.

2-5. Remove the corrugated carton and protective covering and perform a general inspection. Examine the unit for broken controls and indicators and damage to the aluminum case. Retain carton and protective covering until inspection is completed.

2-6. If damage is discovered at this point, report it immediately to the carrier and to Data-Control.

2-7. MOUNTING.

2-8. The unit is designed to be mounted in the GMA, Module Assembly/Power Supply, which has been pre-wired to accept it. Install the unit in the slot designated for it as shown on the wiring diagram (contained in the GMA manual).

CAUTION

The GMA, Module Assembly/Power Supply is wired at the factory to accept the configuration shown by the wiring diagram. If a unit different than that shown on the diagram is plugged in, it is highly unlikely that the unit will operate properly.

2-9. INSTALLATION.

2-10. To install the unit in the GMA, Module Assembly/Power Supply, follow the procedure below.

a. Insert the module into the GMA slot designated for it.
b. Push gently into place until the Elco connectors mesh.
c. If the connectors do not mesh immediately turn the captive screw lightly so as to engage the connectors.
d. When the connectors have meshed, tighten the captive screw to lock the unit into place.

2-11. LUBRICATION.

2-12. The only lubrication required is for the muffin fan contained in the GMA, Module Assembly/Power Supply. Consult the manual on the GMA for details of this procedure.

2-13. COOLING.

2-14. No special cooling procedures are required for this unit.

SECTION III
OPERATION

3-1. GENERAL.

3-2. There are no calibration, adjustment or operating procedures other than monitoring of input and output signals for the basic unit. Optimization of the balance for the data and reference carrier feedthrough components may be realized by following the procedures outlined in Section IV, Theory of Operation.

3-3. CONTROLS & INDICATORS.

3-4. There are no front panel controls located on the basic unit. An optional 12 position switch is provided for programming up to 11 internal crystal reference oscillators.

3-5. Monitor jacks are located on the front panel and are listed in Table 3-1.

Table 3-1. Monitoring Points.

Jacks	Function
INput	Monitors the input frequency.
OUTput	Monitors the reference output frequency to the reference discriminator.
REFerence	Monitors the data output frequency translator.
GRounD	Ground

3-6. INITIAL PROCEDURE.

3-7. Install the unit as described in section II. Apply power to the GMA. The unit is now in operation.

3-8. Monitor the reference input level at the front panel monitor point to make certain that the reference tone is present.

3-9. Make certain that the peak-to-peak output voltage does not exceed the maximum specification.

$$V_{out} = 20\left[\frac{1}{f_{kHz}}\right]^{1/3}$$

where f_{kHz} = the reference frequency in kHz.

The spurious signal noise floor levels will be increased beyond the specification limits when the maximum permissible output voltage level is exceeded. The output level may be controlled by R32 (input level adjustment potentiometer) or by controlling the level of the source connected to the SDC data inputs (Pins 1 and 2).

SECTION IV
THEORY OF OPERATION

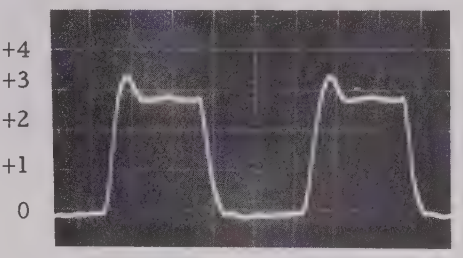
4-1. GENERAL.

4-2. The theory of operation will be described for the basic balanced modulator without options. This configuration is shown in a block diagram form in Figure 4-1. The circuitry is on a single printed circuit board (021463) and contains four basic stages:

a. Input reference limiter.
b. Divided by N programmable frequency dividers.
c. Balanced modulator.
d. Output driver.

4-3. INPUT REFERENCE LIMITER.

4-4. The active limiter section consists of a fast differential voltage comparator, IC1 (Signetics NE529K). Input reference frequencies may be sine waves, triangular or square wave in characteristics. Variations in the symmetry of the input reference waveforms, and any perturbations resulting from input offset voltages and current within IC1 are compensated for by adjustments of R13 and R47. Potentiometer R13 balances the input offset voltages and currents of IC1, while R47 may be used to compensate for asymmetry in the incoming reference voltage wave. The high speed differential comparator chip has a nominal response time of 20 nanoseconds. The amplifier's output is TTL compatible. A typical voltage wave is given below in Figure 4-2.



Horizontal: 100 nanoseconds/division.
Figure 4-2. Limiter Stage, Typical Output Waveform.

4-5. The simplified schematic of IC1 and the associated elements of the limiter stage are shown in Figure 4-3.

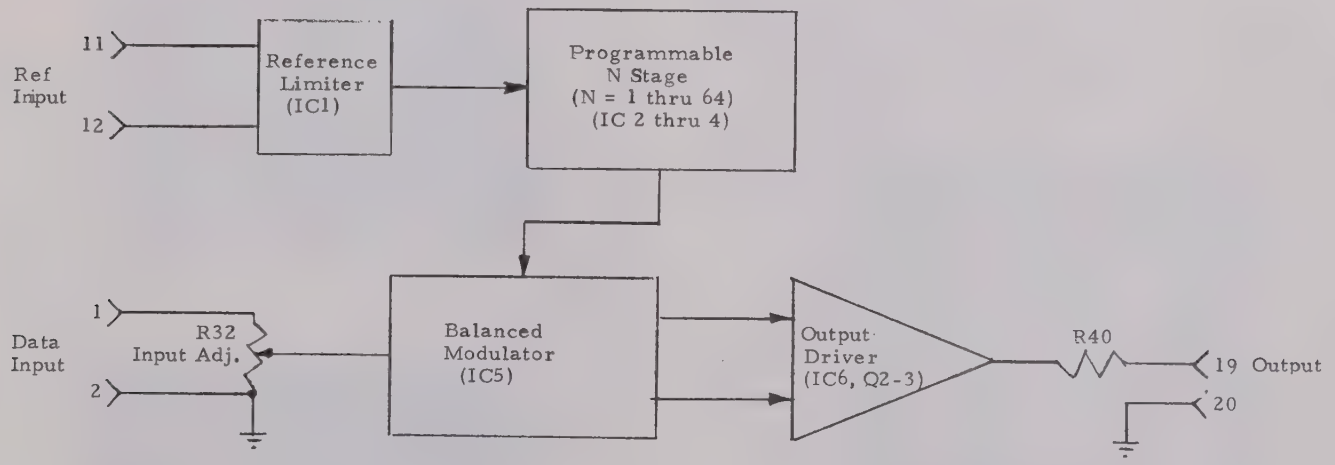


Figure 4-1. Balanced Modulator (021463).

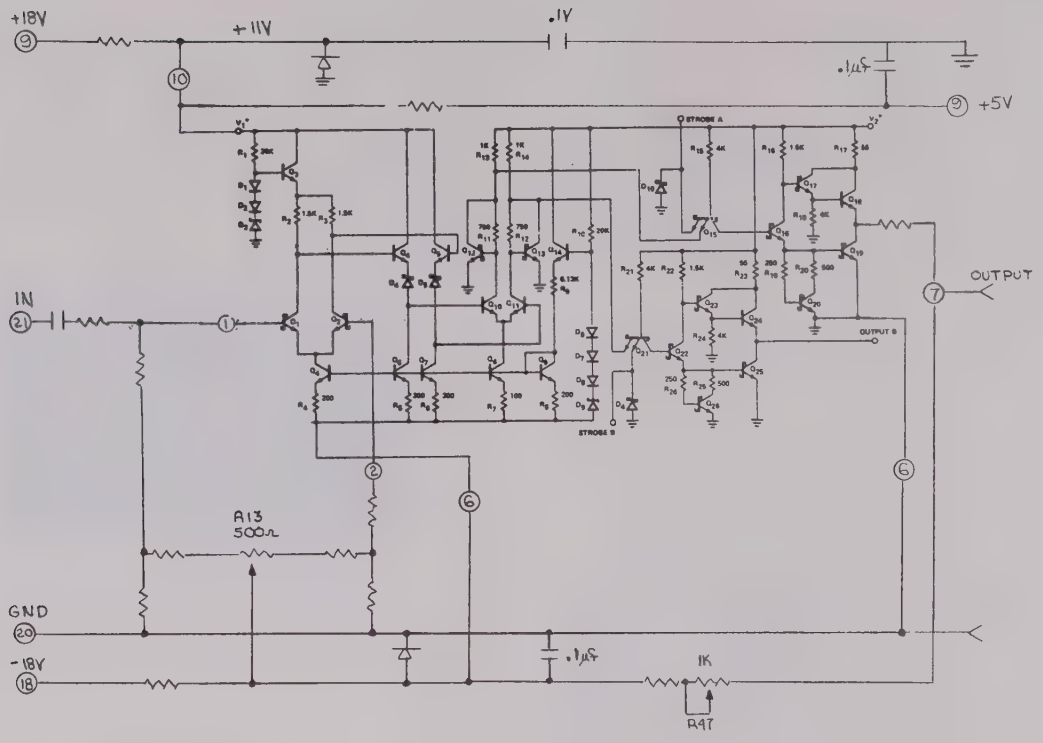


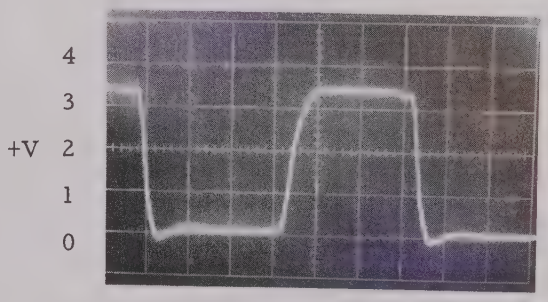
Figure 4-3. Input Reference Limiter, Simplified Schematic.

4-6. DIVIDED BY N PROGRAMMABLE FREQUENCY DIVIDER.

4-7. Frequency divider stages IC2, IC3 and IC4 provide a programmable frequency division in binary increments from 1 to 64. The use of frequency division makes it possible to utilize stable crystal oscillators in the optimum frequency range of 1.5 MHz to 10 MHz for lower frequency reference carrier requirements. Oscillator crystals below 1.5 MHz exhibit significantly poorer characteristics for accuracy, temperature stability and Q factors.

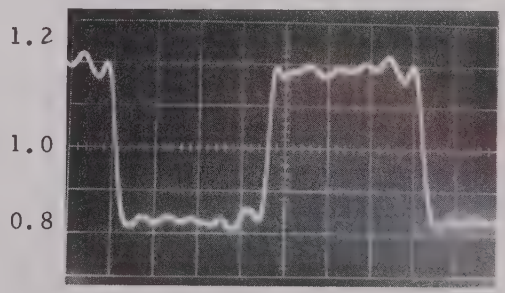
4-8. The binary division is accomplished through the use of three dual D-type edge triggered digital flip-flops. In the divide by 1 mode of operation, the clock input to each of the 6 flip-flop stages is connected through a solder bridge to its respective "preset" input. Frequency digision from 2 to 64 is obtained by unbridging the preset connections, following the stages to operate as normal flip-flop devices.

4-9. A high speed dual D flip-flop (SN74S74) is used as the final stage of the frequency divider to provide extremely fast switch waveforms into the balanced modulator reference input. Typical voltage wavefroms for the SN7474 and the high speed SN74S74 divider stages are shown below in Figures 4-4 and 4-5, respectively.



Horizontal: 50 nanoseconds/division

Figure 4-4. Divider/Driver Stage Outputs IC2, P8/6, IC3, P8/6.



Horizontal: 20 nanoseconds/division

Figure 4-5. High Speed Divider/Driver Output IC4 Test Point 1 (TP1).

4-10. BALANCED MODULATOR.

4-11. The frequency translation of the basic modulator is accomplished by a silicon integrated circuit (MC1596 monolithic balanced modulator). The operation of the integrated circuit's performance may be characterized as that of a double throw, double pole switch begin operated at the rate of the reference frequency as shown in the equivalent circuit diagram of Figure 4-6.

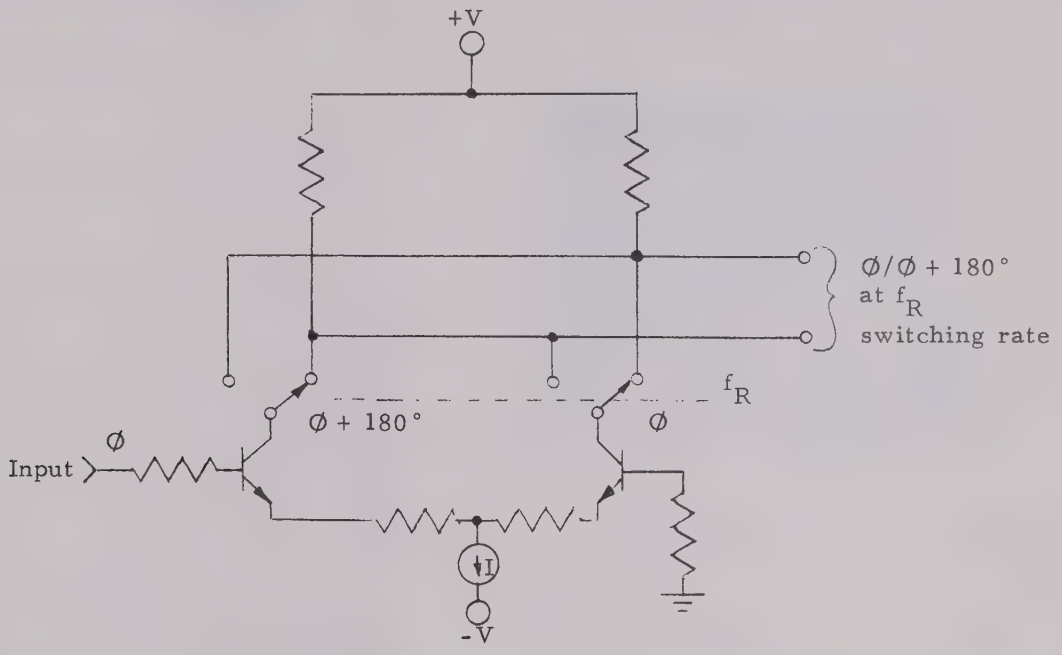


Figure 4-6. Balance Switching Modulator Equivalent Circuit

4-12. The actual switching is accomplished by two pairs of fast transistor switches. The switching characteristics of the modulator generate the typical higher order sideband structure associated with a square wave function. Figure 4-7 illustrates how these higher order sidebands follow the frequency and amplitude distribution of a symmetrical switching square wave. The fundamental and the odd harmonic carriers are present with their modulation sidebands. The levels of the higher odd harmonic carriers of a square wave signal decrease at a rate of 6 dB/octave.

J_0 = 0 dB

J_3 = -9.4 dB

J_5 = -13.98dB

J_7 = -16.9 dB

J_9 = -19.1 dB

This distribution is clearly shown in Figure 4-7.

NOTE

These higher order sidebands must be removed by filtering if they present an interference problem in subsequent RF transmissions of multiplexing applications.

4-13. The frequency spectrum of Figure 4-7, with its unbalanced carrier, will generally be used only for amplitude modulation requirements where residual carrier energy is required for ease of subsequent AM detection.

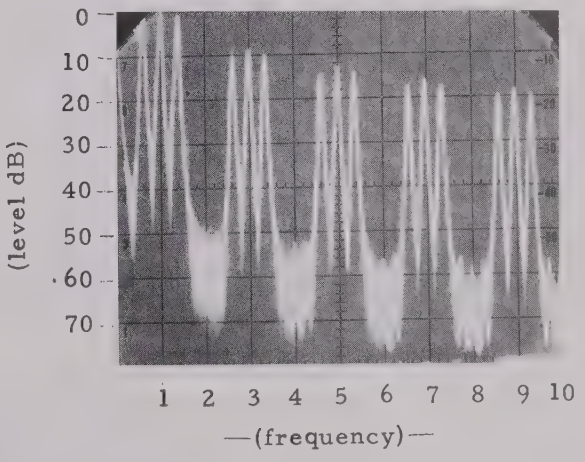


Figure 4-7. Frequency Spectrum of Modulator with unbalanced carrier.

4-14. For applications requiring frequency translation, the carrier should be balanced

to a null as shown in Figure 4-8. For most applications, the desired product will be the lower sideband below the nulled carrier (at approximately 0.6 on Figure 4-8), in which case all other products may be removed by a low pass filter. Other applications may dictate the use of a the higher sideband above the nulled carrier (at approximately 1.4 on Figure 4-8) in which case a bandpass filter would be required to remove the unwanted products. The carrier balance (null) control potentiometer is R37. This control is adjusted for a carrier null condition on all standard units.

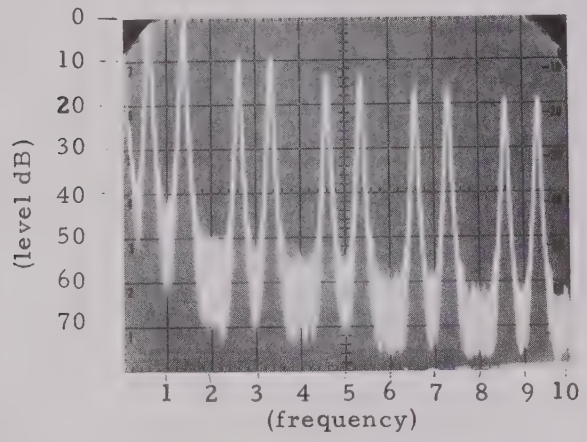


Figure 4-8. Frequency Spectrum of Modulator with a Balanced (Nulled) Carrier.

4-15. The suppression of the higher order even harmonics of the fundamental reference frequency to the extent shown in Figure 4-8 above requires that the pulse symmetry of the reference waveform into the balanced modulator (test point T, of IC5) be better than 0.1%. Figure 4-10 shows the spectrum resulting from a 1% asymmetry of the input reference waveform. The even order harmonics can be seen to be present at a level which is 1% (-40 dB) of the fundamental. Not shown in Figure 4-10, but also present at a level which is -40 dB down from the fundamental, is the fundament data carrier input. Suppression of the data feedthrough and the even harmonics of the reference carrier are then directly related to the reference symmetry.

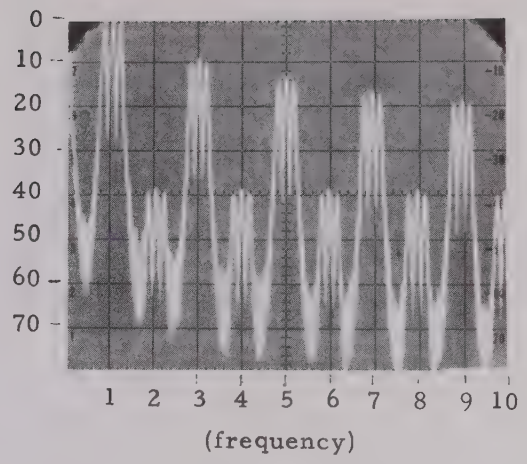


Figure 4-10. Even Harmonics of reference carrier resulting from a 1% asymmetry of the reference carrier.

4-16. For those applications where the reference carrier frequency is divided by a factor of 2 or greater in the N programmable stage, the pulse symmetry will automatically be preserved to better than 1% by the flip-flop action of IC4. When IC2, IC3 and IC4 are used as buffer stages without frequency division, the symmetry of the reference waveform is adjusted better than 1% through the use of R47 and R13 balance potentiometers.

NOTE

These adjustments are made during factory test and setup. There should be no need to readjust these balance potentiometers in the field unless IC1 or IC2 are replaced (reference maintenance, section V).

4-17. OUTPUT DRIVER STAGE.

4-18. The output stage of the balanced modulator is made up of a pair of push-pull drivers (Q2 and Q3) which are capable of being loaded by long coaxial cables, or large capacitive loads. The output impedance of the driver is determined by R40 and is usually selected as 50 ohms. Q4 is a current driver for the push-pull pair which improves the performance of the stage at the higher frequencies. IC_6 is a

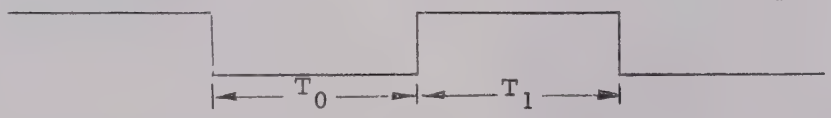


Figure 4-9. Reference Waveform at T_1

$$Nf_0 = V_{DATA} = 20 \text{ LOG } \left| \frac{T_0 \pm T_1}{100} \right|$$

Where: Nf_0 = the level in dB of the even harmonics of the fundamental reference carrier.

V_{DATA} = level in dB of the data feedthrough signal appearing at the output of the modulator.

high speed differential input operational amplifier. Each of the two differential outputs from the balanced modulator circuit (IC5) are combined by IC6 and amplified with a closed loop gain of approximately 28 dB.

4-19. For applications requiring direct current (DC) nulling or offsetting the DC offset control (R24) may be utilized. The adjustment is normally set to 0.0 ±10 millivolts during final test and setup.

SECTION V
MAINTENANCE

5-1. GENERAL.

5-2. This section contains general test procedures and fault isolation procedures.

5-3. TEST EQUIPMENT REQUIRED.

5-4. The equipment required for the tests outlined in this section is listed in Table 3-1.

Table 5-1. Test Equipment

Qty.	Equipment	Model
2	Test Oscillators	HP651A
1	Wave Analyzer	HP310A
1	Spectrum Analyzer*	HP8553L
1	Oscilloscope	Tektronix 454
1	RMS Meter	HP410A

* To be used only on those units to be used at reference frequencies above 1.5 MHz.

5-5. GENERAL TESTS.

5-6. The general qualitative performance of the balanced modulator may be quickly checked utilizing two HP651A, Oscillators, and a Tektronix 454, Oscilloscope, in the test configuration shown below in Figure 5-1.

5-7. When the oscilloscope is triggered externally from the data input frequency, the scope display should clearly show the 180° phase shifting of the input data. Figure 5-2 illustrates typical waveforms for the oscilloscope external trigger being actuated by the data input. Since the displayed waveform is different for high and low frequency reference carriers, a 100 kHz carrier and a 1.5 MHz carrier are shown.

5-8. Triggering the oscilloscope's horizontal sweep from the reference carrier frequency will allow the switching characteristics of the modulator to be displayed. Figure 5-3 shows the typical switched waveforms for both high frequency and low frequency reference carriers. In the expanded time base scale of the high frequency in Figure 5-3a, the switching times can be seen to be approximately 150 nanoseconds. This reflects the 2 MHz response of the output amplifier.

5-9. The linearity of the phase switching can be displayed on a standard 454 oscilloscope using the device in the XY mode of operation. When the output of the modulator is connected to the X axis input and the data input is connected to the Y axis input, the resulting Lissajous shows the amplitude linearity, 0/180 degree phase accuracy, the carrier balance and the data balance. Figure 5-4 represents modulators adjusted for balanced carrier outputs.

5-10. FAUL T ISOLATION TESTING.

5-11. When a modulator fails or when its performance is suspected, the tests and checks described in the following paragraphs should be performed.

5-12. OUTPUT SIGNAL LEVEL. The peak-to-peak output of the balanced modulator should not exceed the maximum limits defined by

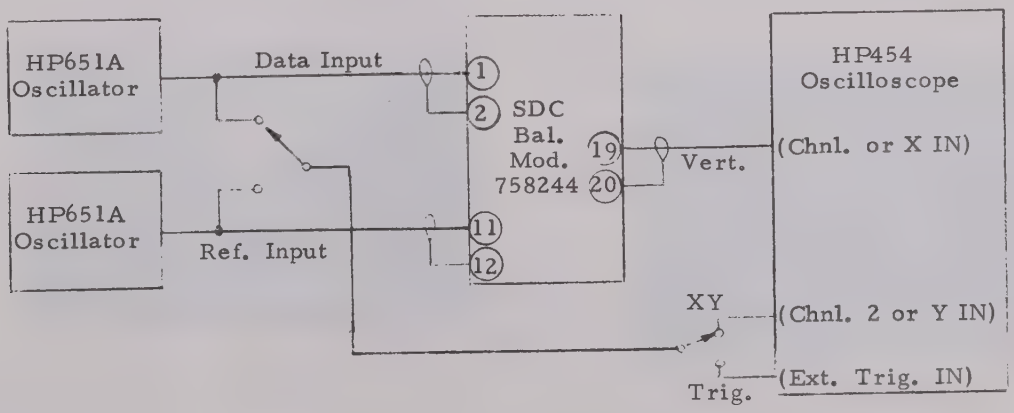


Figure 5-1. General Test Setup

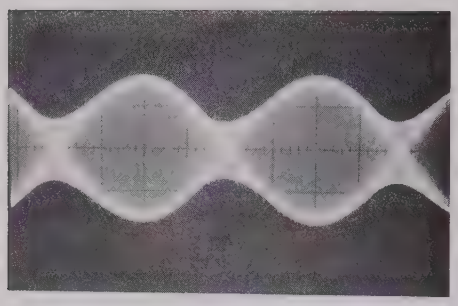


Figure 5-2a. Data Trigger, 1.5 MHz Reference, 1 MHz Data Suppressed Carrier

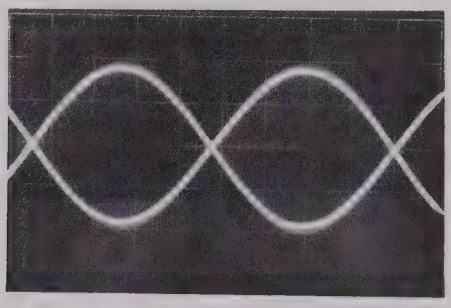
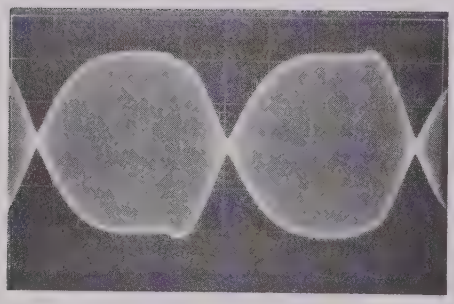
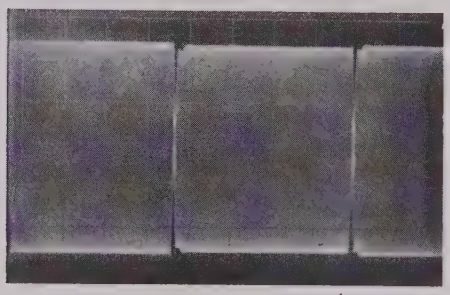


Figure 5-2b. Data Trigger, 100 kHz Reference, 1 kHz Data Suppressed Carrier



Horizontal: 100 nanoseconds/division

Figure 5-3a. Reference Trigger, 1 MHz Reference, 100 kHz Data



Horizontal: 2 microseconds/division

Figure 5-3b. Reference Trigger, 100 kHz Reference 1 kHz Data

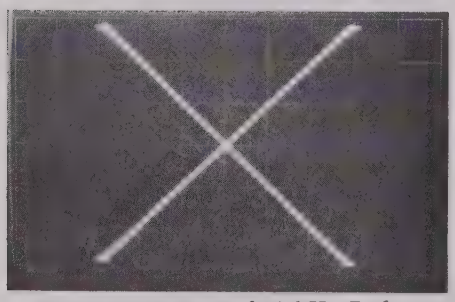


Figure 5-4b. XY Test, 100 kHz Reference, 1 kHz Data

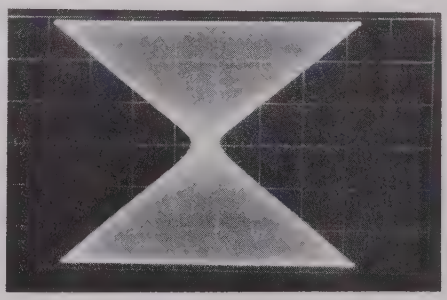


Figure 5-4a. XY Test, 2 MHz Reference, 100 kHz Data

$$V_{P-P}\ \text{Output} = 20\ \text{Log}\ \frac{1}{f_{kHz}}$$ 1/3

These limits are graphically shown in Figure 1-1, Section I. Operation beyond these limits may be permitted provided the spurious signals generated do not fall within portions of the spectrum containing the desired signals.

5-13. SUPPLY VOLTAGES.

a. Plug the modulator board into a standard GMA housing or test fixture and check for the two primary supply voltages.

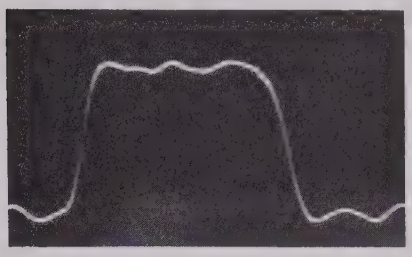
Voltages	Elco#	Board Terminal #
+18V	9	9
-18V	10	10

b. Measure all zener voltages to insure that they are within the limits indicated below:

Zener Voltage	Zener
+ 4V ±1V	CR2/Z2
+ 4V ±1V	CR3/Z3
+ 4V ±1V	CR4/Z4
+11V ±1V	CR1/Z1
+11V ±1V	CR6/Z6
+15V ±1V	CR7/Z7
-15V ±1V	CR5/Z5
- 8V ±1V	CR10/Z10
-15V ±1V	CR11/Z11

5-14. LIMITER RESPONSE.

a. Connect a HP651A, Test Oscillator, to the reference input (terminal 21).
b. Make a note of the unsoldered "divide by" bridges on IC2, IC3 and IC4.
c. Solder all bridges between ÷2, ÷4, ÷8, ÷16 and ÷32.
d. Set the oscillator frequency to 1.5 MHz.
e. Measure the frequency at T_1 and verify that the frequency is 1.5 MHz.
f. Adjust the signal level to -10 dB below 1V RMS (330 mv RMS).
g. Monitor the output of the limiter at test point T_1. The waveform should be similar to that shown below at a 1.5 MHz rate.



+1.35V nominal

+0.8V nominal

10 nanoseconds/div.

T_1 Limiter Output Pulse Response

h. Sweep the oscillator from 11 kHz to 10 MHz. Verify that the waveform at T_1 reproduces the input rate without missing pulses over the entire frequency range.
i. Replace any IC which does not respond correctly over the entire frequency range from 11 kHz to 10 MHz.

NOTE

For those modulators operating from IC1, IC2 and IC3 as buffer stages, where there is no frequency division, the replacement of either IC1 or IC2 will necessitate the readjustment of the data feedthrough circuitry in the manner described in paragraph 5-17.

5-15. DIVIDE BY 64 LOGIC.

a. Remove the solder bridges betweem ÷2, ÷4, ÷8, ÷16 and ÷32 junctions.
b. Connect HP651A, Test Oscillator, to reference input terminal 21 with a frequency of 1.5 MHz.
c. Measure output reference frequency at T_1 and verify by a reading of 46.875 kHz.

5-16. MODULATOR & AMPLIFIER RESPONSE. (See Figure 5-5)

a. Disconnect the reference input to terminal

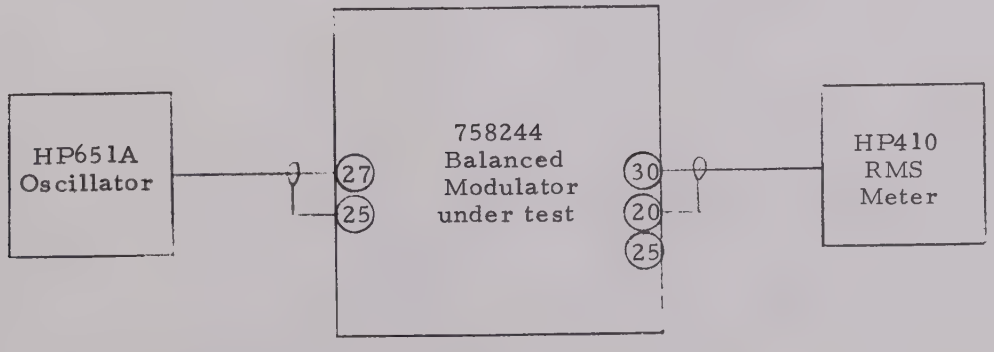


Figure 5-5. Modulator & Amplifier Test Set-up.

(21) of the modulator board.

b. Place a jumper between terminal (21) and ground.

c. Disconnect the data input to terminal (27) of the modulator and connect a HP651A oscillator to the input.

d. Sweep the frequency from 10 kHz to 2 MHz while monitoring the output on pin 30 with a HP410A meter.

5-17. DATA FEEDTHROUGH ADJUSTMENT.

5-18. The reference carrier and data frequencies called out in the paragraphs below will be used for all balanced modulator boards that do not have known or crystal controlled reference carrier frequencies. Those units with specified carrier frequencies will be tested with the following reference and data tones:

	Frequency	Terminal
Carrier frequency:	as specified.	(21)
Data frequency:	60% of specified carrier frequency.	(27)

For those modulators not being used with a specified carrier, a 1.5 MHz reference and a 900 kHz data frequency will be used as described in the following paragraphs:

a. Connect the output of the 651A oscillator to the data input pin, (25), to a frequency of 900 kHz and a level of 200 mv RMS. (For those units with specified reference frequencies, refer to "output voltage level vs. carrier frequency" chart in Figure 1-1, Section I.)

b. Turn data input potentiometer R32 fully clockwise.

c. Adjust the 651A oscillator for a reference frequency into pin (21) to a frequency of 1.5 MHz at a level of 1V RMS (0 dB V).

d. Tune the 310A analyzer of 900 kHz to measure the data feedthrough component. Place a precision decade resistance box across R44 terminals.

e. Place R47 data feedthrough potentiometer to its midpoint range position.

f. Adjust precision decade box on R44 to obtain a data feedthrough null or a level of at least -42 dB. Replace precision decade box with closest 1% resistor.

g. Readjust R47 for minimum null reading on HP310A.

h. Switch the 651A oscillator on the reference input pin (21) to -30 dB V and adjust R13 for a minimum feedthrough reading on the HP310A analyzer (less than 40 dB V).

i. Switch the 651A to -20 dB V and measure feedthrough components. If feedthrough level measures above -40 dB, repeat R13 potentiometer feedthrough null adjustment at the -20 dB V input reference level. Measure feedthrough level at -10 dB V. Again, if feedthrough term is greater than -40 dBV, readjust R13 with input carrier level at -10 dB V.

j. Switch the reference 651A oscillator to an output level of 0 dB V and the 900 kHz feedthrough level measured on the HP310A should be less than 40 dB V.

k. Switch the reference 651A oscillator to +10 dB V, -20 dB V, -30 dB V and -40 dB V. Measure the feedthrough levels.

Reference Carrier	Specification
+10 dB V	-
0	-40 dB down
-10 dB V	-40 dB down
-20 dB V	-
-30 dB V	-

5-19. CARRIER FEEDTHROUGH.

5-20. A carrier frequency of 1.5 MHz will be used for the testing of all balanced modulator boards that do not have specified reference carrier frequencies. Those units having the reference carrier specified will be tested at the specified carrier frequency.

a. Adjust the 651A reference test oscillator to a frequency of 1.5 MHz, with a level into terminal 21 of -10 dB V.

b. Connect the HP310A wave analyzer to the output of the balanced modulator and tune to a frequency of 1.5 MHz.

c. Adjust potentiometer R37 for a minimum output carrier level as measured on the HP310A analyzer. The minimum output carrier level will be less than 0 dB V.

5-21. DC OUTPUT BALANCE ADJUSTMENT.

a. Adjust R24 for an output DC level on terminal (19) of 0V ±0.1V, as measured on the Tektronix 454 oscilloscope.

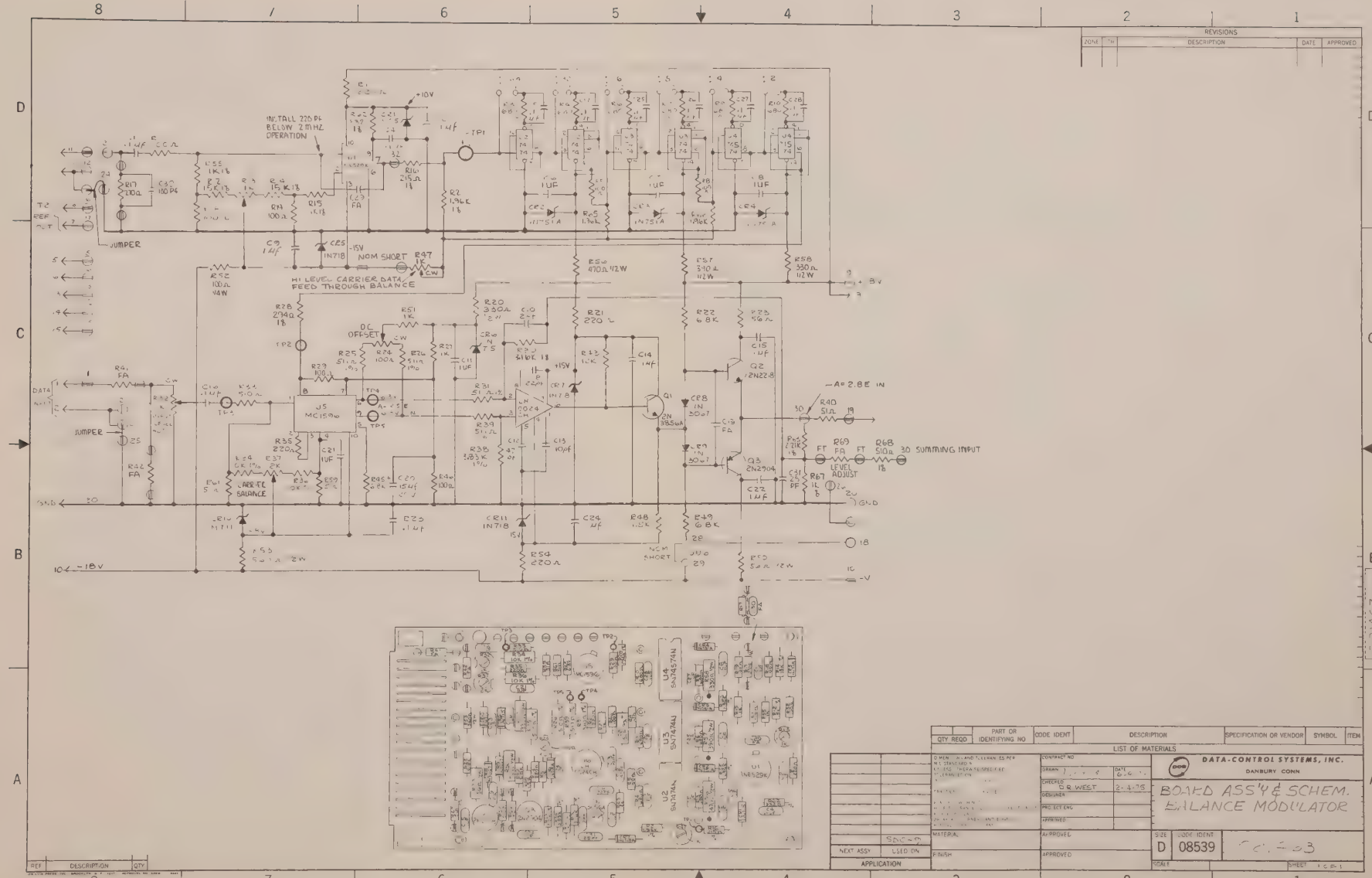
SECTION VI
DRAWINGS

6-1. GENERAL.

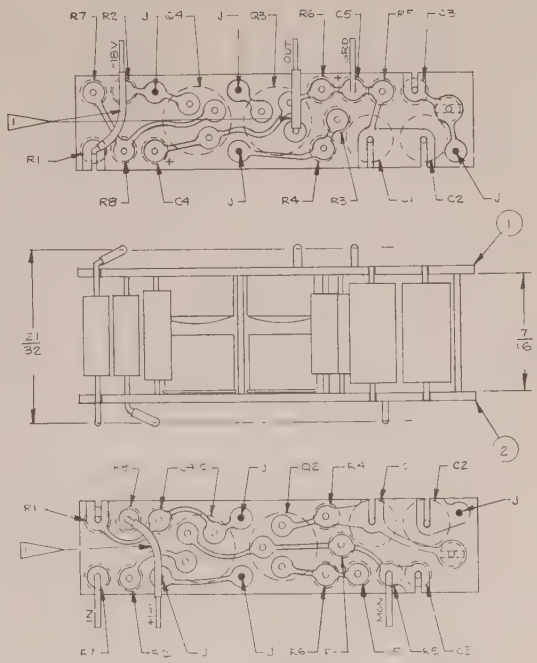
6-2. The drawings contained in this section are furnished to supplement the text.

6-3. DRAWING LIST.

021463	Board Assembly & Schematic
754193	Board Assembly, Oscillator
754207	Board Assembly, Summing Amplifier
758186	Board Assembly, Frequency Divide
756249	Board Assembly, (Reference Oscillator
754021	Board Assembly, Low Pass Filter
021203	Board Assembly, High Pass Filter
020655	Wiring Type (Specific drawing for your unit will be added)


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
INSTALL 220 PF BELOW 2 MHZ OPERATION
JUMPER
HI LEVEL CARRIER DATA FEED THROUGH BALANCE
NOM SHORT
DC OFFSET
CARRIER BALANCE
LEVEL ADJUST
A= 2.8E IN
30 SUMMING INPUT
+8V
-V
GND
10.4 - 18V
LIST OF MATERIALS
QTY REQD | PART OR IDENTIFYING NO | CODE IDENT | DESCRIPTION | SPECIFICATION OR VENDOR | SYMBOL | ITEM
DATA-CONTROL SYSTEMS, INC.
DANBURY CONN
BOARD ASS'Y & SCHEM. BALANCE MODULATOR
SIZE D | CODE IDENT 08539 | 21463
SCALE | SHEET 1 OF 1
REF | DESCRIPTION | QTY
NEXT ASSY | USED ON
APPLICATION

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	K	REDRAWN, P/N ITEM #3 WAS PCA 375-0017-908 & P/N ITEM #7 WAS PCA 375-0006-908 (PACKETIZED)	2/5/68	RJF
	L	CHG ITEM 2 TO 2N4916, ITEM 3 TO 2N3012, ITEM 8 WAS 2K NOM., ITEMS 3 THRU 8, 16 & 18 WERE 1%	12/3/68	
	M	ITEMS 3 THRU 8, 16 & 18 WERE 1%, REMOVED NOTE 4 (AB 5% RES. MAYBE USED	2-13-70	



NOTES:
1. TEFLON SLEEVE & BEND LEADS APPROX AS SHOWN.
2. USE #22 AWG. SOLID WIRE FOR JUMPERS (J).
3. TAG LEADS AS SHOWN (-18V, GRD. ETC.)

5 2N3012 MAY BE USED IN PLACE OF ITEM #13.

QTY REQD	PART OR IDENTIFYING NO	CODE IDENT	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM
1	CB 1/4		RESISTOR, 1/4W 5% 5.6K	A.B.	R7	18
1	150D685X0020A2		CAPACITOR, 6V, 20% 6.8UF	SPRAGUE	C5	17
1	CB 1/4		RESISTOR, 1/4W, 5%, 22 K	A.B	R8	16
						15
2	2N3646		TRANSISTOR		Q3, Q4	14
5 2	2N4916		TRANSISTOR		Q1, Q2	13
1	150D105X0035A2		CAPACITOR, 35V, 20% 1UF	SPRAGUE	C4	12
1	SCM 33 02 J		5% 3300PF (FA)	SCIONICS	C3	11
1	SCM 22 02 J		5% 2200PF (FA)	SCIONICS	C2	10
1	SCM10D472J		CAPACITOR, 5% 4700PF (FA)	SCIONICS	C1	9
1	CB 1/4		RESISTOR, 1/4W, 5% 270 Ω	A.B	R6	8
1	"		10K	"	R5	7
1	"		1K	"	R4	6
1	"		47K	"	R3	5
1	"		1.5K	"	R2	4
1	CB 1/4		RESISTOR, 1/4W, 5% 100 Ω	A.B	R1	3
1	754174		BOARD SUB-ASSY			2
1	754165		BOARD SUB-ASSY			1

LIST OF MATERIALS

754193

REF	DESCRIPTION	QTY

NEXT ASSY	USED ON
	SCF
APPLICATION	

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED TOLERANCES ON:
.XXX ± — .XX ± —
FRACTIONS ± 1/64 ANGLES ±
FLATNESS WITHIN
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX

MATERIAL —
FINISH —

CONTRACT NO
DRAWN J.K. BURLINSON 5-20-65
CHECKED T.L. 6-28-65
DESIGNER J.K. BURLINSON 7-1-65
PROJECT ENG M. GATTI JR. 10-4-65
APPROVED
APPROVED
APPROVED

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

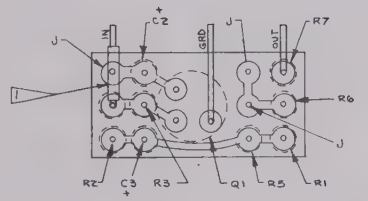
OSCILLATOR BOARD ASSEMBLY

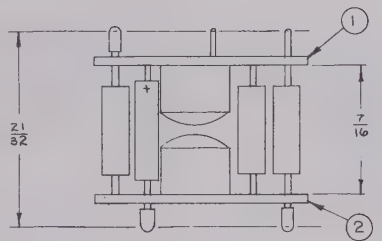
SIZE	CODE IDENT	
C	08539	754193

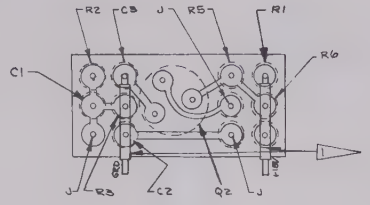
SCALE 1/1 SHEET —

GRAPHIC CONTROLS CORP. BROOKLYN, N. Y. 11211 REPRODUCTION NO. A4000

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	L	REDRAWN	2-26-65	







NOTES:

1. TEFLON SLEEVE & BEND LEADS APPROX AS SHOWN.
2. USE #22 AWG SOLID WIRE FOR JUMPERS (J)
3. TAG LEADS AS SHOWN (+18V, GRD, ETC.).
4. FACE POLARITY MARKS ON COMPONENTS TOWARDS BOARD WHERE MARKS ARE INDICATED.
5. ALLEN BRADLEY 1/4W, 10% RESISTORS MAY BE SUBSTITUTED FOR ELECTRA RESISTORS PROVIDING LEADS ARE TIN PLATED PRIOR TO ASSEMBLY.

754207

QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT.	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM
1	MS5C-D-470-F		RESISTOR 1/4W, 1% 470Ω	ELECTRA	R7	11
1	MF5C-D-562-F		RESISTOR 1/4W, 1% 562Ω	ELECTRA	R6	10
2	2N3646		TRANSISTOR		Q1,Q2	9
1	330-000X5P068BOK		CAPACITOR, 68PF, 100VDC, 10%	ERIE	C1	8
1	150D108X0020A2		CAPACITOR, 1UF, 20VDC, 20%	SPRAGUE	C3	7
1	150D104X0020A2		CAPACITOR .1UF, 20VDC, 20%	SPRAGUE	C2	6
2	MF5C-D-2211-F		RESISTOR 1/4W, 1%, 2.21K	ELECTRA	R2,R5	5
1	MF5C-D-1001-F		RESISTOR 1/4W, 1%, 1K	ELECTRA	R3	4
1	MF5C-D-100-F		RESISTOR 1/4W, 1%, 100Ω	ELECTRA	R1	3
1	754195		BOARD SUB-ASS'Y			2
1	754194		BOARD SUB-ASS'Y			1

LIST OF MATERIALS

REF.	DESCRIPTION	QTY.

NEXT ASSY	USED ON
	SCF-7
	SCF-6A
	SCF-6
	SCF-4
	SCF-2

APPLICATION

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED
TOLERANCES ON:
.XXX ± .010 .XX ±
FRACTIONS ± 1/64 ANGLES ±
FLATNESS WITHIN
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX

MATERIAL —

FINISH —

CONTRACT NO.

		DATE
DRAWN	R J F	6-10-65
CHECKED	T.L.	6-28-65
DESIGNER	J K B	7-1-65
PROJECT ENG	M A P	11-10-65
APPROVED		

APPROVED

APPROVED

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

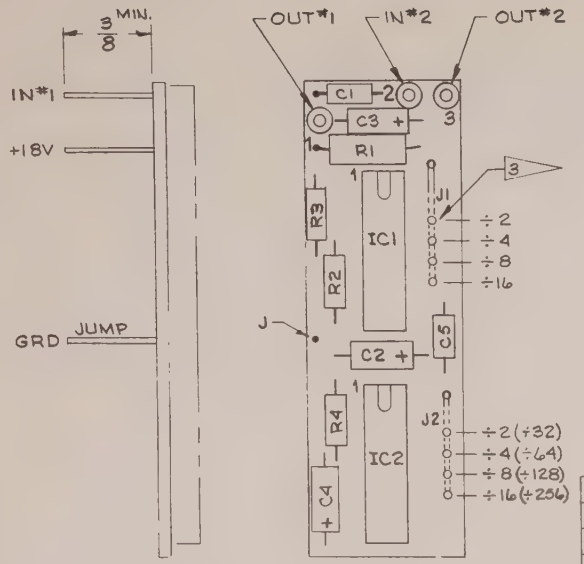
SUMMING AMPLIFIER BOARD ASSEMBLY
SCF

SIZE	CODE IDENT.	
C	08539	754207

SCALE: 4:1 SHEET

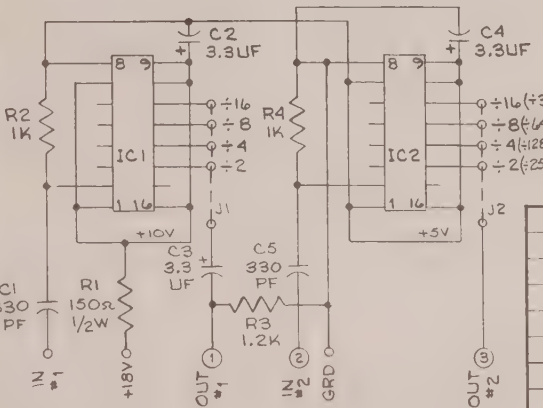
DABLYN PRESS, INC., BROOKLYN, N.Y. 11217 REPRODUCTION NO 4400M ####

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



NOTES:

1. STAMP ASS'Y No. IN 1/8 HIGH CHARACTERS, AS SHOWN, USING BLACK INDELIBLE INK.
2. 'J' DENOTES JUMPER, USE #22 AWG SOLID WIRE.
3. INSTALL JUMPER STRAP IN DIVIDE BY HOLE CALLED OUT ON SPECIAL COMPONENT SHT. OF UNIT USED ON. 'J1' DENOTES F.D.*1, 'J2' DENOTES F.D*2. WHEN DIVIDE BY IS ÷32 OR MORE, JUMPER TERM.*1 TO TERM.*2.
4. SUBSTITUTE: P/N F931659, MFR-FAIRCHILD



QTY REQD	PART NO.	CODE IDENT	DESCRIPTION	VENDOR	SYMBOL	ITEM
2	SN7416IN [4]		INTEGRATED CIRCUIT	T.I. [4]	IC1 & IC2	7
1	CB 1/4		RESISTOR 1/4W, 10% 1.2K	A.B.	R3	6
2	CB 1/4		1/4W, 1K		R2 & R4	5
1	EB 1/2		RESISTOR 1/2W, 10% 150Ω	A.B.	R1	4
3	150D335X0015A2		CAPACITOR 15V, 20% 3.3UF	SPRAGUE	C2, C3 & C4	3
2	SCM10D331J		CAPACITOR 50V, 5% 330PF	SCIONICS	C1 & C5	2
1	758185		BD. DETAIL			1

LIST OF MATERIALS

MULTIPLE	SCF's
NEXT ASSY	USED ON
APPLICATION	

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL—3 PLACE ± .005
DECIMAL—2 PLACE ± .010
FRAC. ± 1/64 ANG. ± .0°30'
FLATNESS WITHIN /IN.
MAT'L
FINISH

CONTRACT NO.
DRAWN — DATE 11-3-72
CHECKED
DESIGNER
PROJECT ENG. — DATE 11-3-72
APPROVED
APPROVED

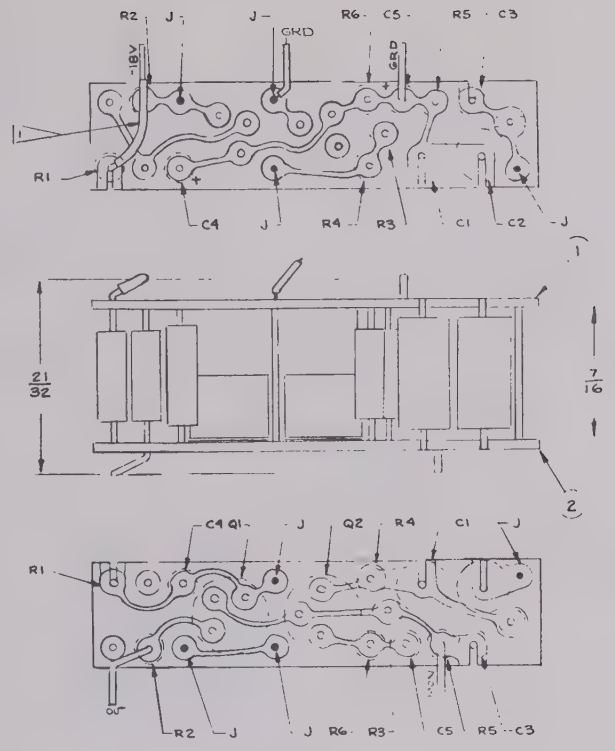
DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

BOARD ASS'Y & SCHEMATIC FREQ. DIVIDE ÷2 THRU ÷16 (x2)

SIZE	CODE IDENT NO	
B	08539	758186

SCALE 2X — SHEET

	A	R1 WAS 2K NOM. F.A. Q1 & Q2 WAS 2N3012.	7/68 GNF
	B	REMOVED ITEMS 16 & 17 ITEM 4 WAS 1.5K	4-30-69 GNF



NOTES:
1. TEFLON SLEEVE & BEND LEADS APPROX. AS SHOWN.
2. USE #22 AWG. SOLID WIRE FOR JUMPERS (J).
3. TAG LEADS AS SHOWN (-18V, GRD. ETC.)
4. ALLEN BRADLEY 1/4W, 10% RESISTORS MAY BE SUBSTITUED FOR ELECTRA RESISTORS PROVIDING LEADS ARE TIN PLATED PRIOR TO ASSEMBLY.
5. 2N3012 MAY BE USED IN PLACE OF ITEM #13.

1	150D685X0006A2	CAPACITOR 6V, 20% 6.8UF	SPRAGUE	C5	17	
					16	
					15	
					14	
5 2	2N3012	TRANSISTOR		Q1, Q2	13	
1	150D105X0035A2	CAPACITOR, 35V, 20% 1UF	SPRAGUE	C4	12	
1	SCM10D392J	5% 3900PF (F.A.)	SCIONICS	C3	11	
1	SCM10D222J	5% 2200PF (F.A.)	SCIONICS	C2	10	
1	SCM10D472J	CAPACITOR 5% 4700PF (FA)	SCIONICS	C1	9	
4 1	MF5C-D-274-F	RESISTOR, 1/4W 1% 274Ω	ELECTRA	R6	8	
1	MF5C-D-1002-F	1% 10K		R5	7	
1	MF5C-D-1001-F	1% 1K		R4	6	
1	MF5C-D-4752-F	1% 47.5K	ELECTRA	R3	5	
1	MS35350	10% 560Ω		R2	4	
1	MF5C-D-2001-F	RESISTOR 1/4W, 1% (100 NOM.) F.A.	ELECTRA	R1	3	
1	754174	BOARD SUB-ASST			2	
1	754165	BOARD SUB-ASST			1	

-1

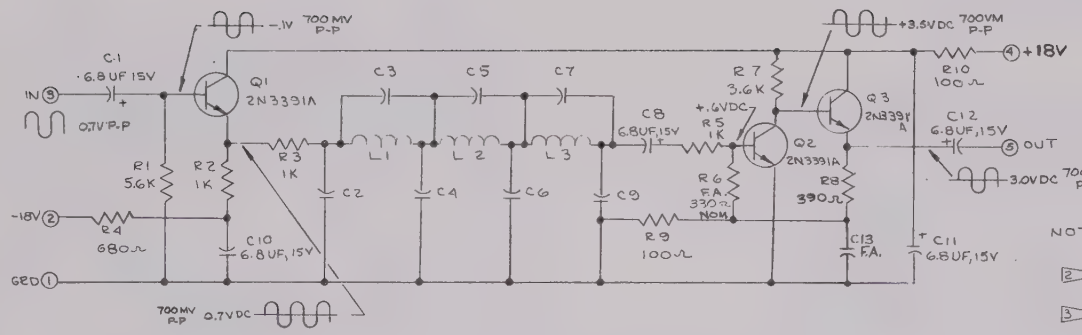
756429

OSCILLATOR(REF.)
BOARD ASSEMBLY

756429

10668 EDC-7R
SCF-3R

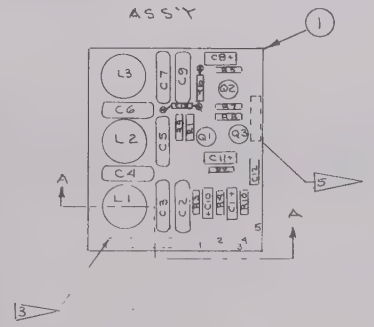
		CHG'D Q3 FROM 2N3319A TO 2N3391A	3-27-68
		ITEM 12 WAS C12	11-13-69
		R6 WAS 1K FA NOM.	7-7-70
	C	DWG. No. WAS 756321	9-6-72
	D	INCORP. CAS639. R10 WAS 100Ω	3-23-73



NOTES:

1. ASSEMBLE PER DCS SPEC AS832011-5000
2. FOR VALUES OF ITEMS #11 & #10 SEE SPECIAL COMPONENT SHEET OF UNIT USED ON.
3. STAMP P/N APPROX AS SHOWN IN 1/8 HIGH BLOCK CHARACTERS, USING WHITE INDELIBLE INK
4. INSTALL ITEM #2 UNDER ALL TRANSISTORS.
5. STAMP FREQ PER SPECIAL COMP SHEET IN 1/8 HIGH CHARACTERS APPROX. AS SHOWN, USING WHITE INDELIBLE INK.

ASS'Y



	1	MS35350-72		RESISTOR, 1/4W, 10% 390Ω		R8	13
	1			CAPACITOR F.A.		C13	12
2	7			CAPACITOR		C2-C7&C9	11
2	3			COIL		L1-L3	10
	3	2N3391A		TRANSISTOR		Q1-Q3	9
	5	150D685X0015B2		CAPACITOR, 15V, 20% 6.8UF	SPRAGUE	C1,8,10,11&12	8
	1	MS35350		RESISTOR, 1/4W, 10% 330Ω F.NOM		R6	7
	1	-58		100Ω		R9	6
	2	-78		680Ω		R4&R10	5
	3	-82		1K		R2,3,5	4
	2	MS35350-100		RESISTOR 1/4W 10% 5.6K		R1&R7	3
4	3	A10042		TRANSIPAD	POSS		2
	1	756320		BOARD SUB-ASS'Y			1

SECTION A-A

[illegible]	11-21-67
[illegible]	11/22/67
[illegible]	11/27/67
R E Light	12-17-71

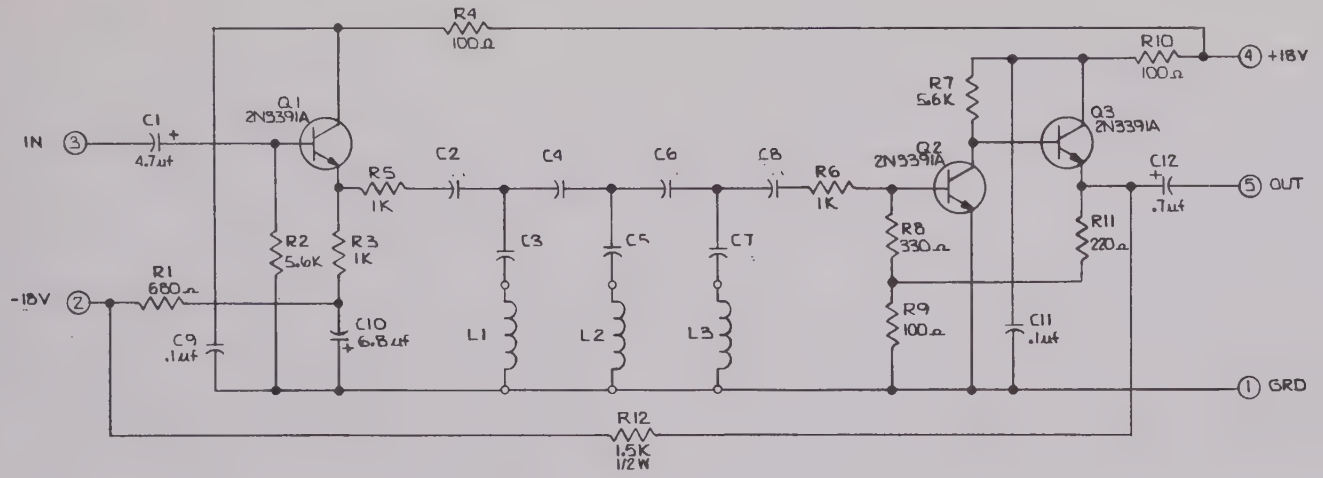
BOARD ASS'Y
LOW PASS FILTER

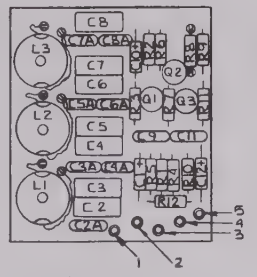
MULTIPLE

754021

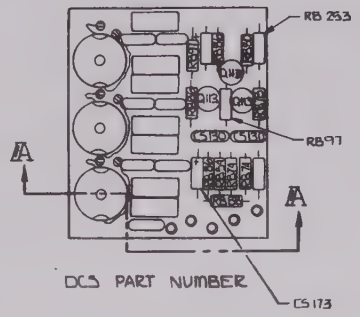
AIU'S CAL

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

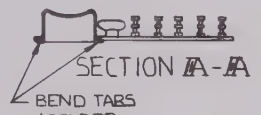




CIRCUIT SYMBOL



DCS PART NUMBER



QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT.	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM

LIST OF MATERIALS

REF	DESCRIPTION	QTY

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED TOLERANCES ON:
.XXX ± .XX ±
FRACTIONS ± ANGLES ±
FLATNESS WITHIN
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX

MATERIAL
FINISH

NEXT ASSY: SDC-8
USED ON
APPLICATION

CONTRACT NO.

		DATE
DRAWN	R BISCOE	2/27/70
CHECKED		
DESIGNER		
PROJECT ENG	G.A.M	2/27/74
APPROVED		2/27/74
APPROVED		
APPROVED		

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

BOARD ASSY & SCHEMATIC
HIGH PASS FILTER

SIZE	CODE IDENT	
C	08539	021203

SCALE SHEET

021203
B

GRAPHIC CONTROLS CORPORATION Buffalo, New York Printed in U.S.A. REPROVEL NO. 440H

REV

SDC-9 Series

P. C 388. SDC-9-R01 388-000-002

Type 004 Wiring Diagram 022900

Common Parts:

388-001-000 includes Z-021463 Bal Mod. Bd.

Special Componets:	Qty per unit
758336 Xtal Board Assy	1
AD20766 -6 Front Panel	1
Xtal 2048 000Khz	1

X-401

Z-754021-1 L. P. F. qty one per unit

Remarks: ÷ 2 on Bal. Mod. Board

Core Mat'l: 14 mm

E-182 Core N28 A400 3 per unit

E-13 Adjust

E-7 Bobbin M 1

E-10 Flange

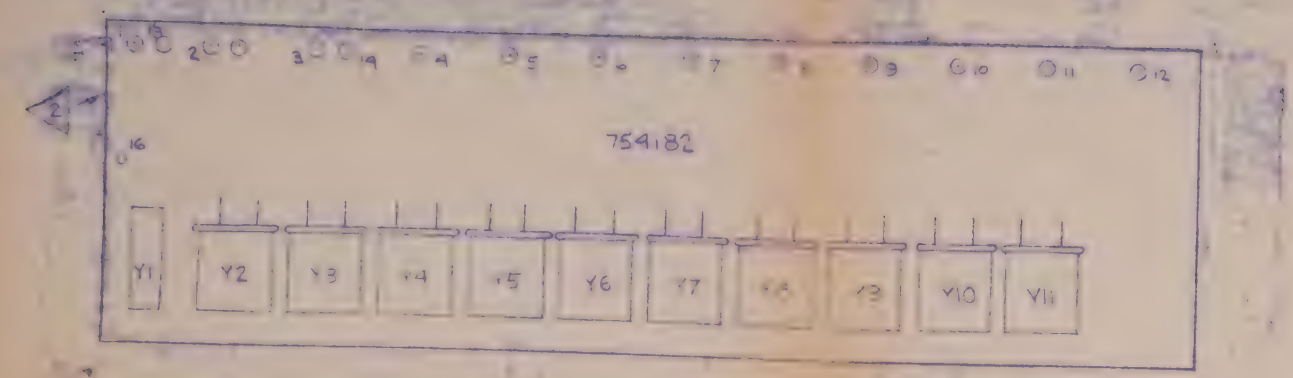
E-9 Mpunt

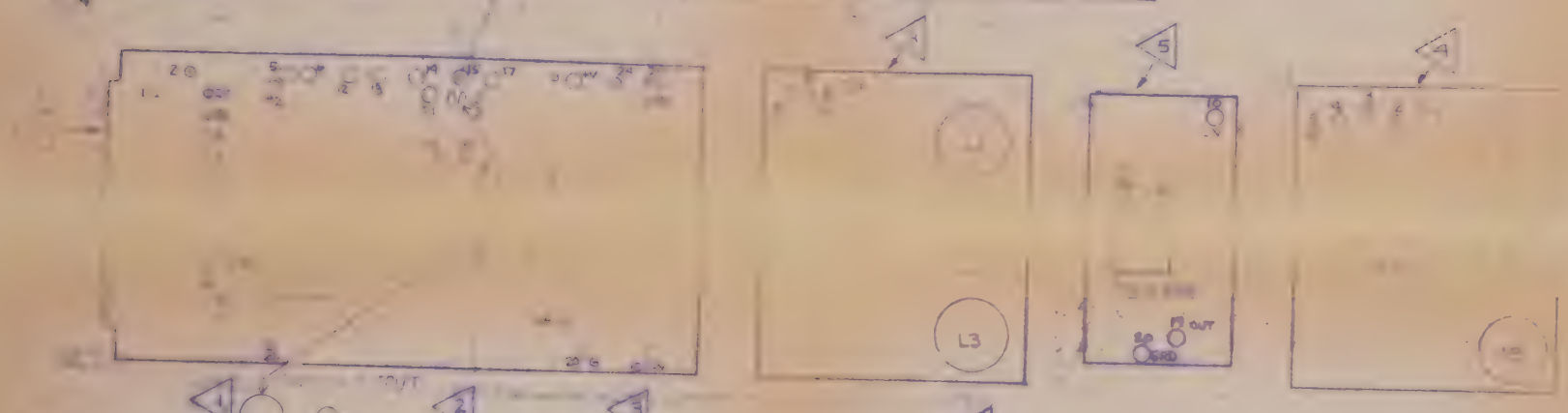
Capacitors: 1 each per unit 3 pe r unit

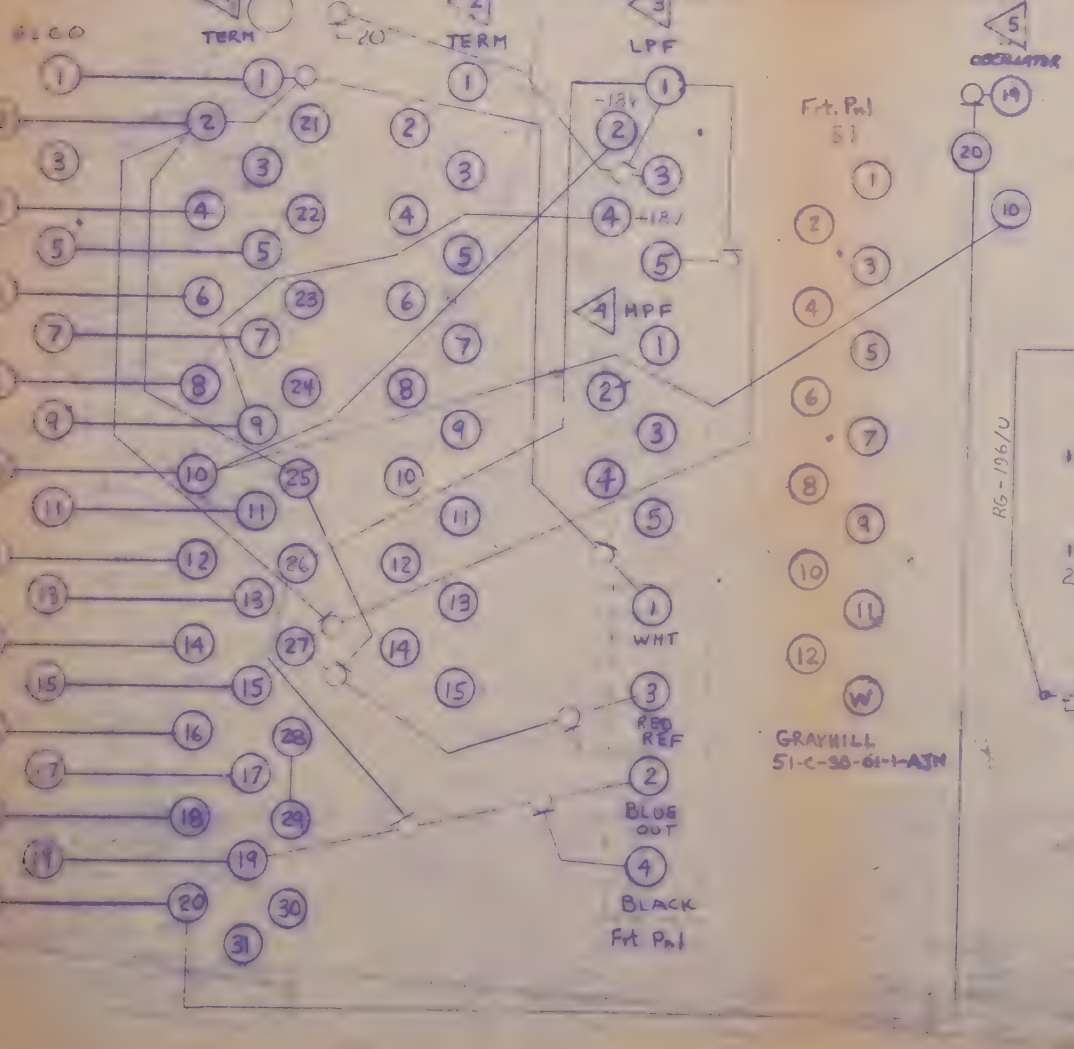
CE-734	169 pf	C2
CE-19	20 pf	C3
CE-89	226 pf	C4
CE-726	107 pf	C5
CE-81	196 pf	C6
CE-715	76.8 pf	C7
CE-731	127 pf	C9

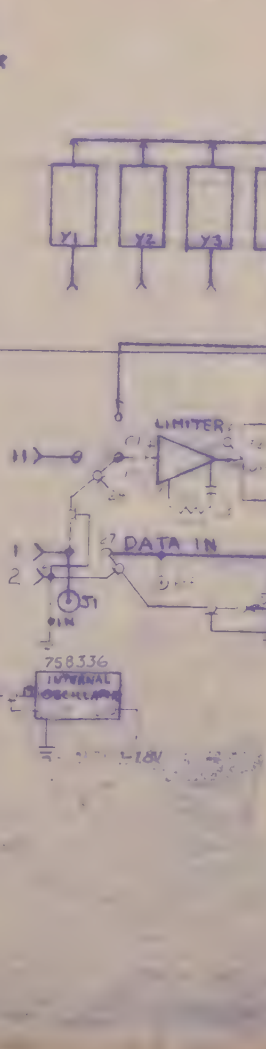
SDC-9-R01 Type 004 Wiring Diagram 022900 Pg 1 of 2

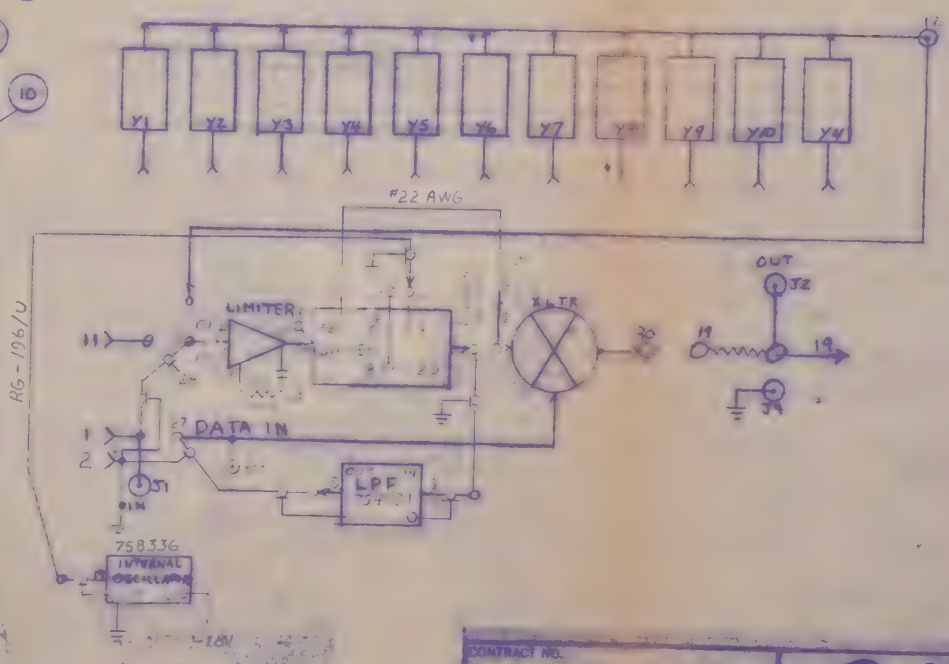
CODE IDENT. NO.	SIZE			REV.
08539	A		022901	
SCALE			SHEET 1 of 2	











CONTRACT NO.	DATA-CONTROL SYSTEMS, INC. DANBURY, CONN.
DRAWN	WIRING DIAGRAM SDC-[illegible] P.C. MOTHERBOARD
CHECKED	
ENGINEER	
PRODUCTION ENG.	08530
APPROVED	

REV

SDC-9-R01 Type 005 Wiring Diagram 023541 Page 1 of 1

SDC-9 SERIES

P. C. 388 SDC-9-R01 388-000-003

Type 005 Wiring Diagram 023541 -

Common Parts:

214-020-000 Common

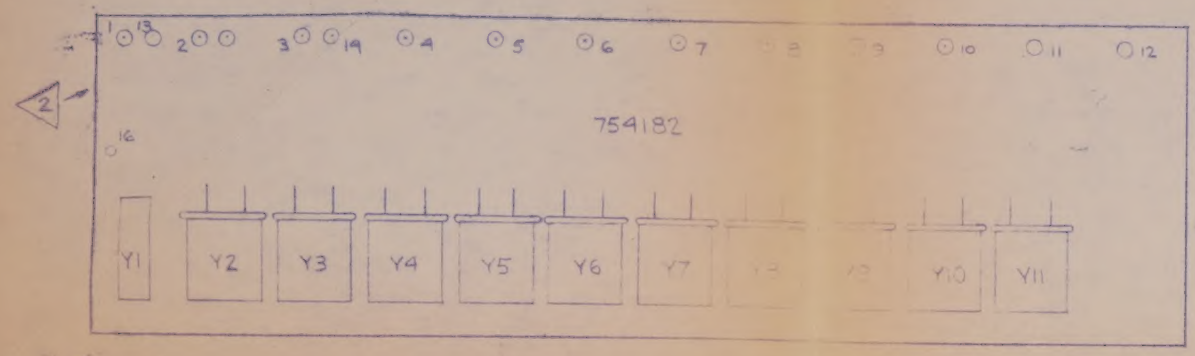
388-001-000 Includes X-021463 Bal Mod. Bd.

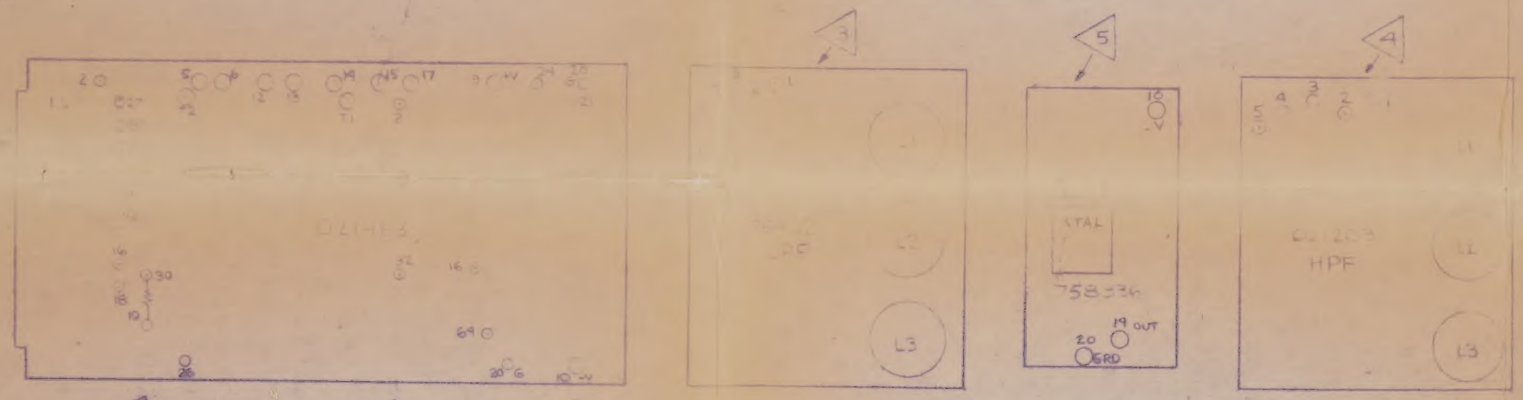
Special Componets:	Qty per unit
758336 Xtal Board Assy	1
AD207665-6 Front Panel	1
Xtal 1700.000 Khz	
X-486	1

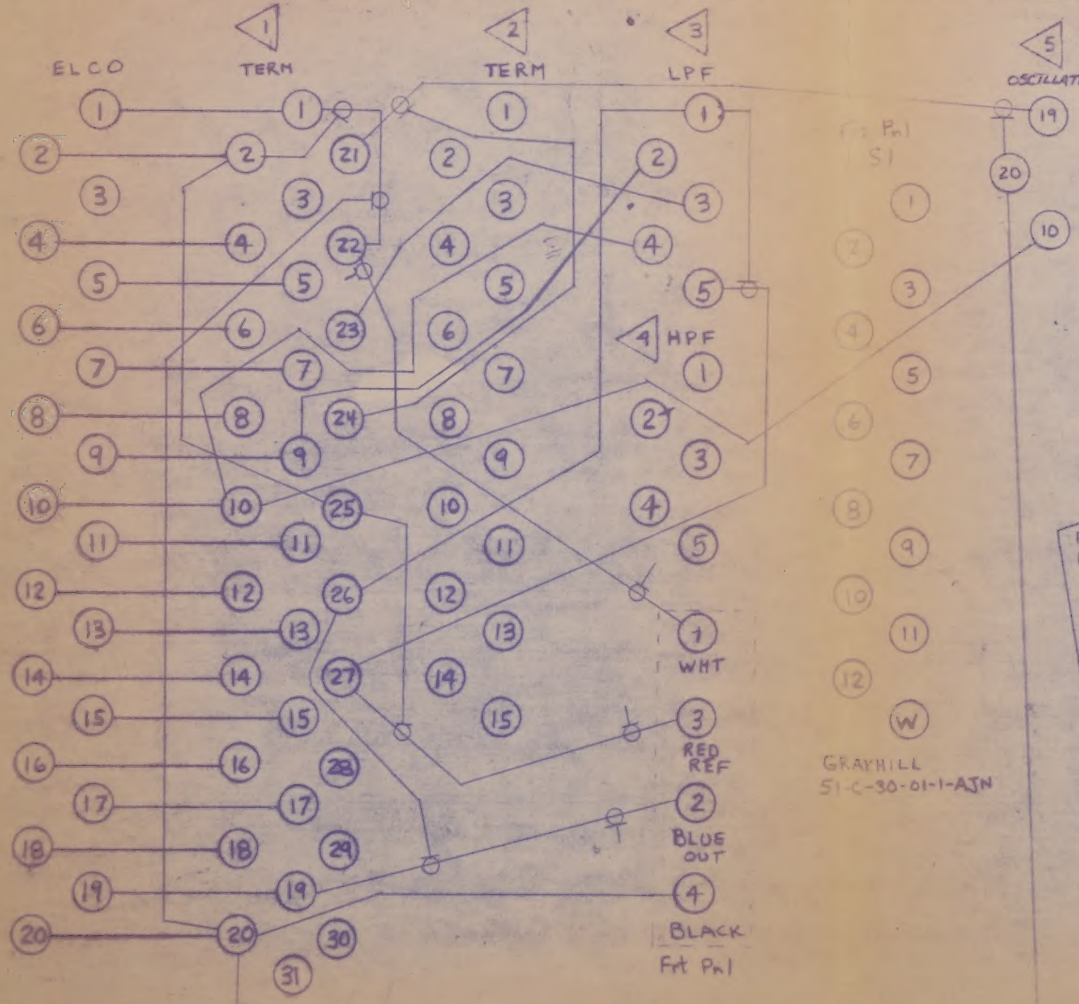
Remarks: No divide Bal. Mod Bd.

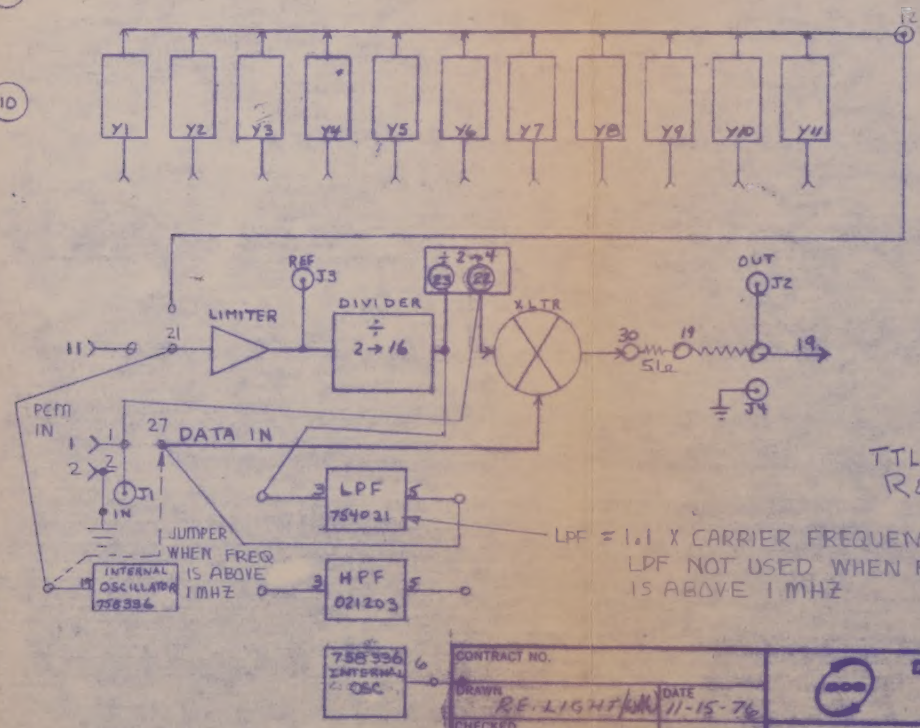
Changed from 022900 to 023541 9-26-78 per REL

CODE IDENT. NO.	SIZE			REV.
08539	A		022901	
SCALE			SHEET 1 of 1	









CONTRACT NO.	
DRAWN R.E. LIGHTFOOT	DATE 11-15-76
CHECKED	
DESIGNER	
PROJECT ENG	
APPROVED	
APPROVED	
APPROVED	

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

WIRING DIAGRAM
SDC-9 R0-1
BI-PHASE MODULATOR

SIZE | CODE IDENT 08539